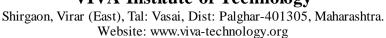
Late Shri Vishnu Waman Thakur Charitable Trust's



VIVA Institute of Technology





Department of Electronics and Telecommunication Engineering

Report on ISTE Approved One Week Short Term Training Program on "VLSI Design & Embedded Systems"

Organized by Electronics and Telecommunication Department

The objective of the VLSI Design & Embedded Systems training program is to address the research, development and design problems and advance their solutions in VLSI circuits for embedded system and widespread computing applications. This STTP provides comprehensive coverage of VLSI Design and its hardware description languages while providing opportunities for Hands-on practical's on FPGA Board & Raspberry Pi.

The purpose of this STTP is to bring together researchers & PG students from academia and Engineers & Scientists from industry and R&D institutes to have discussions on the recent advances in VLSI Design and Embedded systems.

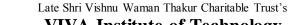
This program also deals with the basic understanding, designing and simulation of the VHDL and Eagle software which will provide practical exposure to the participants. The STTP aims at equipping teachers with skills and knowledge in order to create a better society by guiding, training and motivating the students to take up research projects.

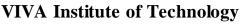
Topics Covered in STTP on "VLSI Design & Embedded Systems"

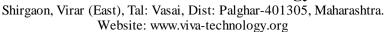
- Basics of VLSI and Introduction to Hardware Description Languages
- Introduction to PLDs FPGA design Classification of IC Technology
- Introduction to Raspberry Pi its features
- Hands on practice Raspberry Pi
- PCB designing using Eagle software
- Embedded systems application.

At the end of STTP participants are able to

- To get familiarized with VLSI Design using VHDL.
- To learn about recent trends of research in field on Raspberry Pi and Arduino.
- After the completion of this course the participants will be able to design schematic and PCB Layout using Eagle software.
- Enhance the basic knowledge of Embedded Systems technology.









Department of Electronics and Telecommunication Engineering

The University of Mumbai introduced revised curriculum which includes, VLSI Design and Microcontroller and Microprocessor as compulsory subject for the third year students. As new developments are introducing in industry day by day demanding expertise in the field of Embedded Systems and VLSI Design, it was felt necessary that the teaching faculty also become competent in the said technology. With keeping this as an intension the ISTE approved STTP was conducted from 2nd January to 6th January, 2018 in Electronics and Telecommunication Engineering Department, VIVA Institute of Technology.

Details of the speakers is as under

SN.	Name of the Guest	Details of the Speaker	Topics Addressed	Date
	Speaker			
1	Mr. Rajendra Babar	Assistant Professor, Sinhgad Institute of Technology, Lonavala	Basics of VLSI and Introduction to Hardware Description Languages Behavioural Modeling & Structural Modeling Hands on practice - FPGA board	02/01/2018
2	Mr. Rajendra Babar	Assistant Professor, Sinhgad Institute of Technology, Lonavala	Introduction to PLDs FPGA design Classification of IC Technologies Testing of Logic circuits Hands on practice – FPGA board	03/01/2018
3	Mr. Abhilash Panicker	Assistant Manager, RS Components and Control LTD, Mumbai	Introduction to Raspberry Pi Its features Hands on practice – Raspberry Pi	04/01/2018
4	Mr. Nayan Mistry	Founder and CTO NMtechnocraft, Mumbai.	Basics of Embedded systems & recent trend PCB designing using Eagle software	05/01/2018

Participants were the teaching faculty of Engineering College. Total of 14 faculty members participated in the One week Short Term Training Program conducted.

On the last day of STTP institute had received the feedbacks from the participants that they have learned and enhanced their knowledge in this STTP and they would always want to attend this kind of STTP in this institute once again. The overall feedback of the Training Program was encouraging and was highly rated by the participants.