Sample Questions

Computer Engineering / Artificial Intelligence and Data Science / Artificial Intelligence and Machine Learning / Computer Science and Engineering (Artificial Intelligence and Machine Learning) / Computer Science and Engineering (Data Science) / Computer Science and Engineering (Internet of Things and Cyber Security Including Block Chain Technology) / Cyber Security / Data Engineering / Internet of Things (IoT)

Subject Name: Microprocessor **Semester: IV**

Multiple Choice Questions

	Choose the correct option for following questions. All the Questions are compulsory and carry equal marks
1.	In protected mode of 80386, the VM flag is set by using
Option A:	IRET instruction or task switch operation
Option B:	IRET instruction
Option C:	Task switch operation
Option D:	NOP
2.	The instructions that are used for reading an input port and writing an output port respectively are
Option A:	MOV, XCHG
Option B:	MOV, IN
Option C:	IN, MOV
Option D:	IN, OUT
3.	While CPU is executing a program, an interrupt exists then it
Option A:	follows the next instruction in the program
Option B:	jumps to instruction in other registers
Option C:	breaks the normal sequence of execution of instructions

Option D:	stops executing the program
4.	8086 can access up to?
Option A:	512KB
Option B:	1MB
Option C:	2MB
Option D:	256KB
5.	Because of Pentium's superscalar architecture, the number of instructions that are executed per clock cycle is
Option A:	1
Option B:	2
Option C:	3
Option D:	4
6.	The paging unit is enabled only in
Option A:	virtual mode
Option B:	addressing mode
Option C:	protected mode
Option D:	Real Mode
7.	i. In 8257 register format, the selected channel is disabled after the terminal count condition is reached when
Option A:	Auto load is set
Option B:	Auto load is reset
Option C:	TC STOP bit is reset
Option D:	TC STOP bit is set
8.	All the functions of the ports of 8255 are achieved by programming the bits of an internal register called

Option A:	data bus control
Option B:	read logic control
Option C:	control word register
Option D:	Status Register
9.	When non-specific EOI command is issued to 8259A it will automatically
Option A:	set the ISR
Option B:	reset the ISR
Option C:	set the INTR
Option D:	reset the INTR
10.	For a single task in protected mode, the 80386 can address the virtual memory of
Option A:	32 GB
Option B:	64 MB
Option C:	32 TB
Option D:	64 TB
11.	i. The recurrence of the numerical values or constants in a program code is reduced by
Option A:	EQU
Option B:	ASSUME
Option C:	LOCAL
Option D:	LABEL
12.	The hyperthreading technology automatically involves the
Option A:	decrease of die area
Option B:	increase of die area
Option C:	decrease of die area to half
Option D:	increase of die area to half

13.	a. The 80386 enables itself to organize the available physical memory into pages, which is known as
Option A:	segmentation
Option B:	Paging
Option C:	memory division
Option D:	Virtual memory
14.	The number of debug registers that are available in 80386, for hardware debugging and control is
Option A:	2
Option B:	4
Option C:	8
Option D:	16
15.	The instruction, JMP 5000H:2000H; is an example of
Option A:	intrasegment direct mode
Option B:	intrasegment indirect mode
Option C:	intersegment direct mode
Option D:	intersegment indirect mode
16.	The salient feature of Pentium is
Option A:	superscalar architecture
Option B:	superpipelined architecture
Option C:	superscalar and superpipelined architecture
Option D:	multiple instruction issue
17.	The speed of integer arithmetic of Pentium is increased to a large extent by
Option A:	on-chip floating point unit
Option B:	superscalar architecture
Option C:	4-stage pipelines

Option D:	instruction cache
18.	For 8086 microprocessor, the stack segment may have a memory block of a maximum of
Option A:	32K bytes
Option B:	64K bytes
Option C:	16K bytes
Option D:	128K bytes
19.	Which of the following is not a module of Pentium 4 architecture?
Option A:	front end module
Option B:	execution module
Option C:	control module
Option D:	Memory subsystem module
20.	The type of the interrupt may be passed to the interrupt structure of CPU from
Option A:	interrupt service routine
Option B:	Stack
Option C:	interrupt controller
Option D:	Segments
21.	The flag that is used in 8086 for string manipulation instructions is
Option A:	AF
Option B:	ZF
Option C:	DF
Option D:	CF
22.	In 8086 microprocessor one of the following statements is not true.
Option A:	Coprocessor is interfaced in Min mode
Option B:	Coprocessor is interfaced in Max mode
Option C:	20 bit address bus
Option D:	Supports pipelining
23.	The BIU prefetches the instruction from memory and store them in
Option A:	Queue

Option B:	Register
Option C:	Memory
Option D:	Stack
24.	Segment address, Offset address & Physical address are _____ bits each in 8086
Option A:	8, 8 & 16
Option B:	8, 16 & 20
Option C:	16, 16 & 20
Option D:	8, 8 & 8
25.	The OUT DX, AX instruction present in 8086 microprocessor causes?
Option A:	data retrieval from IO device
Option B:	data transfer to memory
Option C:	data transfer to IO device
Option D:	data retrieval from memory
26.	The instruction that unconditionally transfers the control of execution to the specified address is
Option A:	CALL
Option B:	IRET
Option C:	RET
Option D:	JNZ
27.	In PUSH instruction, after each execution of the instruction, the stack pointer is
Option A:	incremented by 1
Option B:	decremented by 1
Option C:	incremented by 2
Option D:	decremented by 2
28.	In DMA if more than one channel requests service simultaneously, the transfer will occur as
Option A:	burst transfer
Option B:	simultaneous transfer
Option C:	Parallel transfer
Option D:	multi transfer
29.	When the SP(active low)/EN(active low) pin of 8259A used in buffered mode, then it can be used as a
Option A:	input to designate chip is master or slave
Option B:	buffer disable
Option C:	buffer enable
Option D:	input to designate chip is master
30.	In 8255, BSR mode is applicable for which port
Option A:	Port A
Option B:	Port B
Option C:	Port C

Option D:	Port A &B
31.	Cascade PIC mode provides maximum how many interrupt levels in 8259
Option A:	8
Option B:	16
Option C:	63
Option D:	64
32.	80386 support which type of descriptor table from the following?
Option A:	TDS
Option B:	ADT
Option C:	GDT
Option D:	MDS
33.	Which control registers of 80386 are associated with paging mechanism?
Option A:	CR0, CR2, CR3
Option B:	CR1, CR2, CR3
Option C:	CR0, CR1 CR2
Option D:	CR0, CR1 CR2,CR3
34.	How many flags are active in flag register of 80386?
Option A:	9
Option B:	12
Option C:	13
Option D:	10
35.	80386 real mode have
Option A:	Only overlapped segments
Option B:	Either overlapped or non-overlapped segments
Option C:	Only nonoverlapped segments
Option D:	Paging
36.	MESI protocol of Pentium comprises of
Option A:	Mutual, Exclusive, Shared, and Invalid
Option B:	Modified, Exhaustive, Shared, and Interactive
Option C:	Modified, Exclusive, Shared, and Valid
Option D:	Modified, Exclusive, Shared, and Invalid
37.	The speed of integer arithmetic of Pentium is increased to a large extent by
Option A:	4-stage pipelines
Option B:	superscalar and superpipelined architecture
Option C:	superscalar architecture
Option D:	on-chip floating point unit
38.	a. In Pentium, the percentage of hits to the total cache access is given by
Option A:	Hit Ratio
Option B:	Accuracy
Option C:	Efficiency

Option D:	Precision
39.	Which of this is not true for Pentium 4?
Option A:	Hyperthreading (HT) gets illusion as if two processors are executing code in parallel
Option B:	Execution trace cache to store 12k micro-operation
Option C:	126 instruction window in instruction pool
Option D:	Data Bus of 32 bit
40.	Hyperthreading uses the concept of
Option A:	Simultaneous multithreading
Option B:	Distributed decoding
Option C:	Multiple switching
Option D:	Pipelining
41.	8086 supports _____ s/w Interrupts
Option A:	2
Option B:	64K
Option C:	256
Option D:	8
42.	After RESET is given to 8086 the content of CS is
Option A:	FFFF0
Option B:	0000
Option C:	FFFF
Option D:	0FFFF
43.	If segment address = FF00 H, offset address = 00FF H, then the physical address is _____
Option A:	FFFF0
Option B:	0FFFF
Option C:	FF0FF
Option D:	FFFFF
44.	In 8086 size of pre fetch queue is
Option A:	6 Byte
Option B:	4 Byte
Option C:	4 Bit
Option D:	2 Byte
45.	In an instruction, generally a destination operand is
Option A:	Only Register
Option B:	Only Memory location
Option C:	Register or Memory location
Option D:	Immediate data
46.	MOV AX, FFFFH will affect

Option A:	All flags
Option B:	No flags
Option C:	CY and AC flags
Option D:	Zero flag
47.	Which of the following instruction is not valid
Option A:	MOV AX,1000H
Option B:	MOV AH, BL
Option C:	MOV DS, 0100H
Option D:	MOV [SI], AX
48.	_____ stores the bits required to mask the IR lines of 8259
Option A:	ISR
Option B:	IMR
Option C:	IRR
Option D:	PR
49.	The bus is available when the DMA controller receives the signal
Option A:	HRQ
Option B:	HLDA
Option C:	DACK
Option D:	INTA
50.	If microprocessor has 10-bits address bus, then it can generate _____addresses.
Option A:	32767
Option B:	25652
Option C:	65536
Option D:	1024
51.	In 8255 strobed input/output mode is
Option A:	Mode 0 of I/O mode
Option B:	Mode 1 of I/O mode
Option C:	Mode 2 of I/O mode
Option D:	BSR mode
52.	Size of page in 80386 is
Option A:	1 Kb
Option B:	2 Kb
Option C:	4 Kb
Option D:	8 Kb
53.	The 80386DX has an address bus of
Option A:	8 address lines
Option B:	16 address lines
Option C:	20 address lines
Option D:	32 address lines

54.	In a selector if table indicator = 1 then it select
Option A:	Local descriptor table
Option B:	Global descriptor table
Option C:	Trap gate
Option D:	Task gate
55.	The control register that stores the 32-bit linear address, at which the previous page fault is detected is
Option A:	CR0
Option B:	CR1
Option C:	CR2
Option D:	CR3
56.	Pentium floating point unit has
Option A:	2 stage pipelines
Option B:	4 stage pipelines
Option C:	8 stage pipelines
Option D:	16 stage pipelines
57.	Due to the branch instruction, the incorrect instruction loaded into pipeline must be discarded. This is called
Option A:	Flushing
Option B:	Bubble
Option C:	Disturbance
Option D:	Wrong entry
58.	What lead to the development of MESI and MEI protocol ?
Option A:	Cache size
Option B:	Cache Coherency
Option C:	Bus snooping
Option D:	Number of caches
59.	P4 has hyper pipelined technology with
Option A:	3 stages
Option B:	5 stages
Option C:	10 stages
Option D:	20 stages
60.	Trace cache can store up to
Option A:	10 K decoded micro operation
Option B:	8 K decoded micro operation
Option C:	12K decoded micro operation
Option D:	4 K decoded micro operation

Descriptive Questions

1	Explain different types of Interrupts? Explain Interrupt Vector table for 8086

2	Draw and explain the internal block diagram of 8257? How DMA operations are performed?
3	Explain what is Branch Prediction Logic in Pentium? Explain working of Branch Prediction with suitable diagram?
4	Compare the 8086, 80386, Pentium Processor.
5	Draw and explain the internal architecture of 80386 microprocessor?
6	Explain the operating modes of 80386?
7	Explain the internal architecture of 8086 microprocessor? Differentiate the functioning of Minimum mode and Maximum mode?
8	Write an assembly language program to find the largest number from an unordered array of 8-bit numbers?
9	Interface 32K word of memory to 8086 microprocessor system. Available memory chips are 16K*8 RAM. Use suitable decoder for generating chip logic.
10	Explain address and data bus demultiplexing in 8086 with diagram.
11	Discuss need for memory banking in 8086
12	Explain mode-0 and mode-2 of 8255
13	Explain interrupt procedure of 8086
14	Explain integer pipeline of Pentium
15	Write a note on Hyperthreading
16	Write 8086 assembly language program to find Even and Odd number from the set of 5 8-bit numbers.
17	Design 8086 system based on the following specifications 1. 16Kb ROM using 8 Kb chips 2. Minimum mode 3. 5Mhz clock
18	Explain protection mechanism of 80386 with diagram.
19	Explain memory segmentation in 8086 with neat diagram.
20	Draw timing diagram of memory read operation in minimum mode.
21	Explain programmer's model of 8086 microprocessor.
22	Explain BSR mode of 8255.
23	Explain Branch Prediction logic with neat diagram.
24	With neat diagram explain Net burst micro architecture of Pentium 4
25	Explain with neat diagram architecture of 80386 microprocessor.
26	Design 8086 microprocessor based system working in minimum mode with the following specifications. I) 8086 microprocessor working at 8 MHz. II) 16 KB EPROM using 8K devices. Clearly show memory map with address range. Draw a neat schematic.
27	Write an 8086 assembly language program to print content of flag register.